Jason Blocklove

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Education

New York University — **Brooklyn, NY**
Ph.D. Candidate — Electrical and Computer Engineering (ABD) — *Present (Expected May 2027)*
Thesis topic: *Leveraging Generative AI for Hardware Design and Security*

Rochester Institute of Technology — **Rochester, NY**
MS — Computer Engineering — *2020*
Thesis: *Hardware Intellectual Property Protection Through Obfuscation Methods*

Rochester Institute of Technology — **Rochester, NY**
BS — Computer Engineering — *2020*
Graduated Magna Cum Laude

Industry Positions

Johns Hopkins University Applied Physics Lab — **Laurel, MD**
Associate Professional Staff 1 - Electrical Engineer — *July 2020 – June 2022*
Developed PCBs, FPGA designs, and embedded systems software focused on DSP

SICOM Systems — **Lansdale, PA**
Research and Development Co-Op — *May 2018 – August 2018*
Integrated high-level languages with subsystem-level Linux constructs
Aided in reverse engineering a custom communication protocol to integrate with legacy system

Johnson & Johnson — **Raritan, NJ**
Computer Engineering Co-Op — *June 2017 – December 2017*
Developed advanced distribution list creation tool in Java

Publications

Journal Articles

[J1] **Jason Blocklove**, Shailja Thakur, Benjamin Tan, Hammond Pearce, Siddharth Garg, Ramesh Karri, "Automatically improving LLM-based verilog generation using EDA tool feedback," *ACM Trans. Des. Autom. Electron. Syst.*, Mar. 26, 2025, issn: 1084-4309. doi: 10.1145/3723876

[J2] **Jason Blocklove**, Hammond Pearce, Ramesh Karri, "Lowering the bar: How large language models can be used as a copilot by hardware hackers," *IEEE Security & Privacy*, vol. 23, no. 5, pp. 27–37, 2025. doi: 10.1109/MSEC.2025.3600140

Peer-Reviewed Conference Proceedings

[C1] **Jason Blocklove**, Siddharth Garg, Ramesh Karri, Hammond Pearce, "Chip-chat: Challenges and opportunities in conversational hardware design," in *2023 ACM/IEEE 5th Workshop on Machine Learning for CAD (MLCAD)*, Sep. 2023, pp. 1–6. doi: 10.1109/MLCAD58807.2023.10299874

[C2] **Jason Blocklove**, Siddharth Garg, Ramesh Karri, Hammond Pearce, "Evaluating LLMs for hardware design and test," in *2024 IEEE LLM Aided Design Workshop (LAD)*, Jun. 2024, pp. 1–6. doi: 10.1109/LAD62341.2024.10691811

[C3] **Jason Blocklove**, Md Raz, Prithwish Basu Roy, Hammond Pearce, Prashanth Krishnamurthy, Farshad Khorrami, Ramesh Karri, "OffRAMPS: An FPGA-based intermediary for analysis and modification of additive manufacturing control systems," in *2024 54th Annual IEEE/IFIP International Conference on De-*

pendable Systems and Networks (DSN), ISSN: 2158-3927, Jun. 2024, pp. 535–543. doi: 10.1109/DSN58291.2024.00057

[C4] **Jason Blocklove**, Steve Farris, Michael Kurdziel, Marcin Łukowiak, Stanisław Radziszowski, "Hardware obfuscation of the 16-bit s-box in the MK-3 cipher," in *2021 28th International Conference on Mixed Design of Integrated Circuits and System*, Jun. 2021, pp. 104–109. doi: 10.23919/MIXDES52406.2021.9497537

[C5] Weihua Xiao, **Jason Blocklove**, Matthew DeLorenzo, Johann Knechtel, Ozgur Sinanoglu, Kanad Basu, Jeyavijayan Rajendran, Siddharth Garg, Ramesh Karri, "Special day – guide: Genai units in digital design education," in *2026 Design, Automation & Test in Europe Conference (DATE)*, 2026, pp. 1–7. doi: 10.23919/DATE69613.2026.11539269

[C6] Prithwish Basu Roy, **Jason Blocklove**, Mudit Bhargava, Hammond Pearce, Prashanth Krishnamurthy, Ozgur Sinanoglu, Nikhil Gupta, Farshad Khorrami, Ramesh Karri, "Scream: Secure channels for real-time evaluation of additive manufacturing," in *Proceedings of the ACM Asia Conference on Computer and Communications Security*, ser. ASIA CCS '26, Bangalore, India: Association for Computing Machinery, 2026, pp. 234–249, isbn: 9798400723568. doi: 10.1145/3779208.3805981 [Online]. Available: https://doi.org/10.1145/3779208.3805981

Invited Talks/Special Sessions with Refereed Publication

[T1] Chandan Kumar Jha, Muhammad Hassan, Khushboo Qayyum, Sallar Ahmadi-Pour, Kangwei Xu, Ruidi Qiu, **Jason Blocklove**, Luca Collini, Andre Nakkab, Ulf Schlichtmann, Grace Li Zhang, Ramesh Karri, Bing Li, Siddharth Garg, Rolf Drechsler, "Large language models (LLMs) for verification, testing, and design," in *2025 IEEE European Test Symposium (ETS)*, ISSN: 1558-1780, May 2025, pp. 1–10. doi: 10.1109/ETS63895.2025.11049311

[T2] Kangwei Xu, Denis Schwachhofer, **Jason Blocklove**, Ilia Polian, Peter Domanski, Dirk Pflüger, Siddharth Garg, Ramesh Karri, Ozgur Sinanoglu, Johann Knechtel, Zhuorui Zhao, Ulf Schlichtmann, Bing Li, "Large language models (LLMs) for electronic design automation (EDA) : Special session paper," in *2025 IEEE 38th International System-on-Chip Conference (SOCC)*, 2025, pp. 1–6. doi: 10.1109/SOCC66126.2025.11235352

Books

[B1] **Jason Blocklove**, Benjamin Tan, Hammond Pearce, Siddharth Garg, Ramesh Karri, *From Quips to Chips*. Springer, 2026, Under contract, submitted for publication.

Preprints (Not Published Elsewhere)

[P1] **Jason Blocklove**, Shailja Thakur, Hammond Pearce, Benjamin Tan, Siddharth Garg, Ramesh Karri, "AutoChip: Automating HDL generation using LLM feedback," arXiv:2311.04887, arXiv, Jun. 4, 2024. doi: 10.48550/arXiv.2311.04887 arXiv: 2311.04887[cs].

Other Publications

[O1] **Jason Blocklove**, "How generative AI can simplify digital hardware design," Microelectronics Packaging & Test Engineering Council (MEPTEC), Tech. Rep., Aug. 2024. [Online]. Available: https://issuu.com/mepcom/docs/meptec_report_summer_2024/17

[O2] **Jason Blocklove**, "Hardware intellectual property protection through obfuscation methods," ISBN: 9798664704785, M.S. Rochester Institute of Technology, United States – New York, 2020, 101 pp.

Other Presentations

October 2026: *IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)* — Short Course – Generative AI for Digital Hardware Design: Conversation Through Automation

July 2026: *IEEE/ACM Design Automation Conference (DAC)* — GREAT Workshop – AI Hardware Attack Challenge

September 2024: *IEEE Embedded Systems Week (ESWEEK)* — Automating Hardware Design with Large Language Models

June 2024: *Microelectronics Packaging & Test Engineering Council (MEPTEC)* — Automating Hardware Design with Large Language Models

May 2024: *IEEE Test Spring School (TSS)* — Tutorial: Automating Hardware Design with Large Language Models – Feedback Loops for Security

March 2024: *IEEE Design, Automation, and Test in Europe (DATE)* — Tutorial: Automating Hardware Design with Large Language Models

September 2023: *ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)* — Tutorial: The Intersection of Hardware, Security, and Large Language Models

Teaching Experience

New York University **Brooklyn, NY**
Instructor of Record *January 2024 – May 2024*
Course: Special Topics – Introduction to Hardware Security

New York University **Brooklyn, NY**
Teaching Assistant *September 2022 – December 2023*
September 2024 – December 2024
September 2026 – Present
Courses:
- Advanced Hardware Design
- Digital Logic and State Machine Design

Rochester Institute of Technology **Rochester, NY**
Laboratory Instructor *January 2019 – May 2020*
Course: Digital System Design II

Rochester Institute of Technology **Rochester, NY**
Curriculum Development Assistant *May 2017 – August 2017*
May 2018 – December 2018
Course: Digital System Design II
Curriculum changes:
- Added new lab exercises to introduce crossing clock domains
- Developed new labs for the complete course to match new lecture curriculum focused on designing a MIPS processor from scratch in VHDL

Rochester Institute of Technology **Rochester, NY**
Teaching Assistant *September 2016 – May 2017*
January 2018 – May 2020
Courses (Graduate):
- Hardware and Software Design for Cryptographic Applications
- Reconfigurable Computer

Courses (Undergraduate):
- Interface and Digital Electronics
- Digital System Design II
- Digital System Design I

Mentorship

Graduate Students

Siddh Javeri: *MS in Computer Engineering at NYU* – Supervised summer research through TREx Program
Thinh Nguyen: *MS in Computer Engineering at NYU* – Supervised summer research through TREx Program
Kahlia Gronthos: *MS in Computer Engineering at NYU* — Supervised capstone project

Undergraduate Students

Youssof Saleh: *BS in Computer Engineering* — Supervised summer research internship
Helin Mazi: *BS in Computer Engineering* — Supervised summer research internship
Fatima Farooq: *BS in Computer Engineering* — Supervised summer research internship

Abay Oralov: *BS in Computer Engineering* — Supervised summer research internship

Club Projects

NYU OSIRIS Lab: Supported PCB design, debugging, and validation for custom CSAW badges for CTF

Outreach

NYU Cybersecurity Awareness Workshop
Organizer and Judge *2023 – 2025*
- Designed challenges for student teams to use generative AI to develop hardware Trojans
- Organized multiple judges from both industry and academia

IEEE HOST
Competition Organizer *2026*
- Created competition for student teams to perform red-team/blue-team hardware security analysis using Generative AI

IEEE DAC
Competition Organizer and Judge *2026*
- Created competition for student teams to use Generative AI to reverse engineer and maliciously modify FPGA bitstreams

Service

To the University

Committees:
2025: *NYU* — Li-Ion Battery Powered Micromobility Device Policy Committee

To the Community

Reviwer: Journal of Systems Architecture (JSA), *ACM Transactions on Embedded Computing Systems (TECS)*, *IEEE Computer Magazine*, *IEEE Transactions on Information Forensics and Security (TIFS)*, *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, *Journal of Hardware and Systems Security*, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, *IEEE International Test Conference (ITC)*, *IEEE/IFIP Dependable Systems and Networks (DSN)*, *International Conference on Compilers, Architectures, and Synthesis for Embedded Systems (CASES)*, *Design, Automation, and Test in Europe (DATE)*, *European Test Symposium (ETS)*, *Design Automation Conference (DAC)*

In the Media

Articles Covering Research

October 2025: *NYU Tandon School of Engineering* — AI tools can help hackers plant hidden flaws in computer chips, study finds [link]

January 2024: *NYU Tandon School of Engineering* — From "Chip Chat" to "Chip In Hand": NYU Tandon researchers fabricate the world's first chip designed through conversations with an artificial-intelligence platform [link]

June 2023: *Tom's Hardware* — Conversation With ChatGPT Was Enough to Develop Part of a CPU [link]

Interview

June 2023: *Zero to ASIC Course* — First chip designed with AI! An interview with Dr. Hammond Pearce and Jason Blocklove [link]